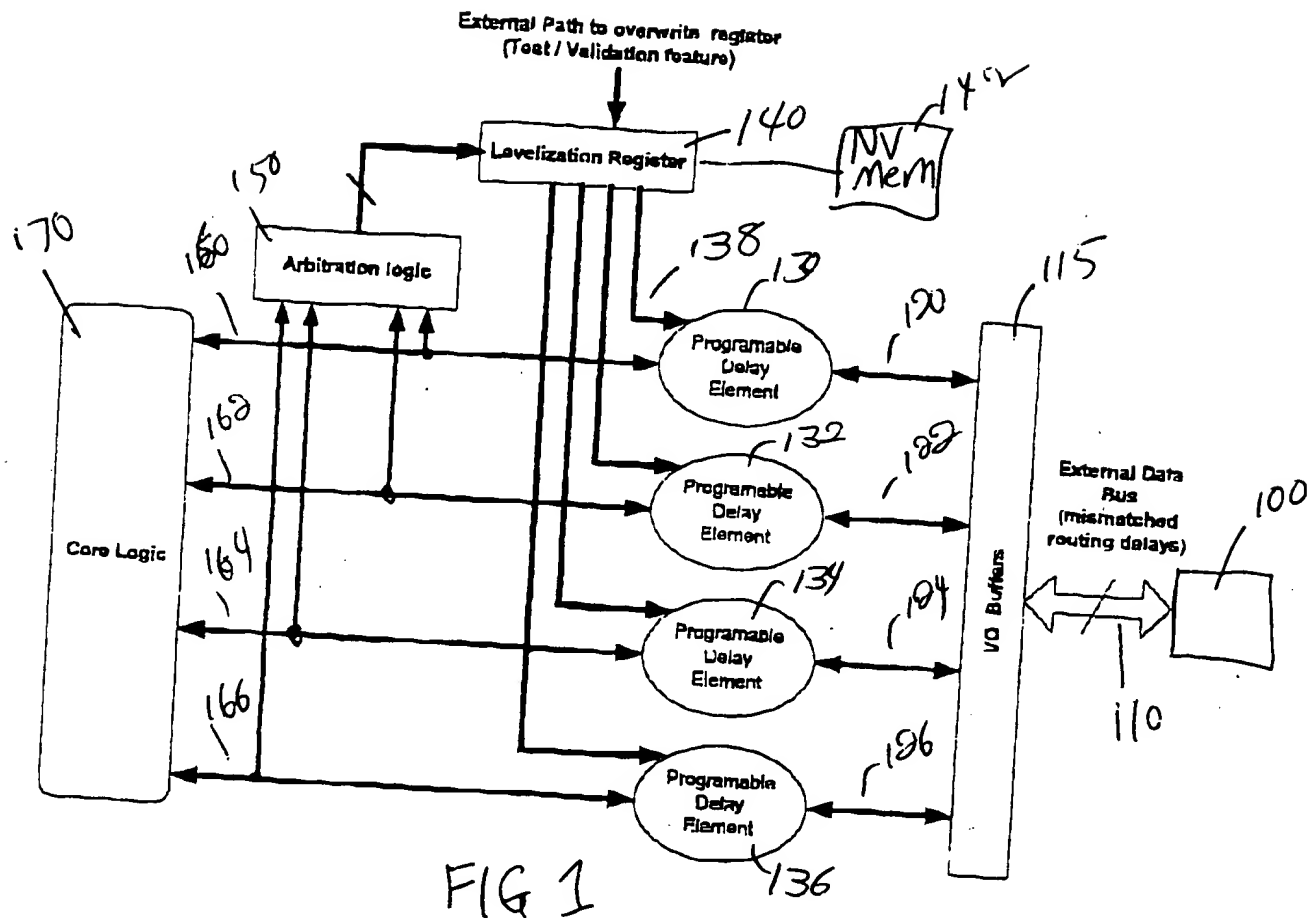


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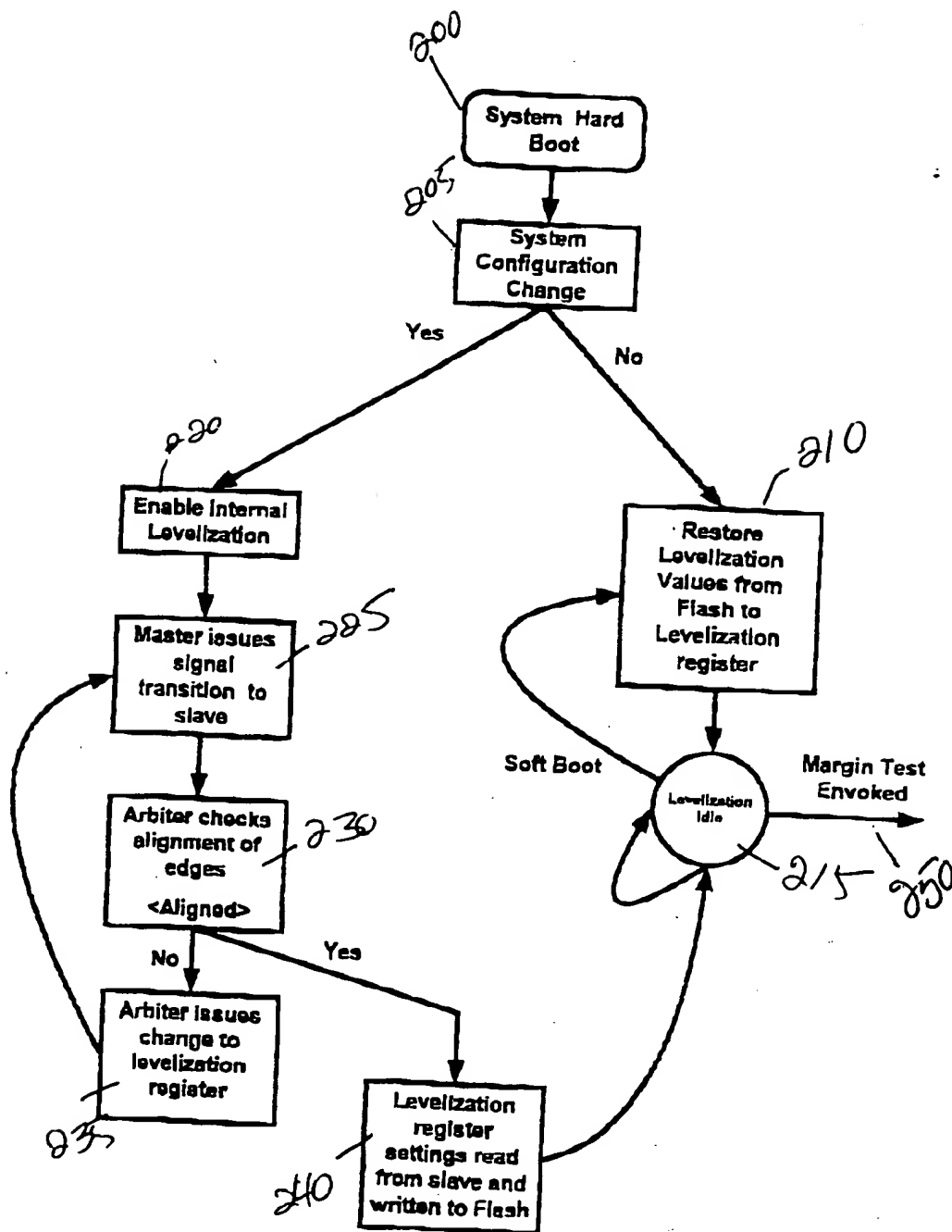


FIG 2

System Margin Testing using line levelization registers.

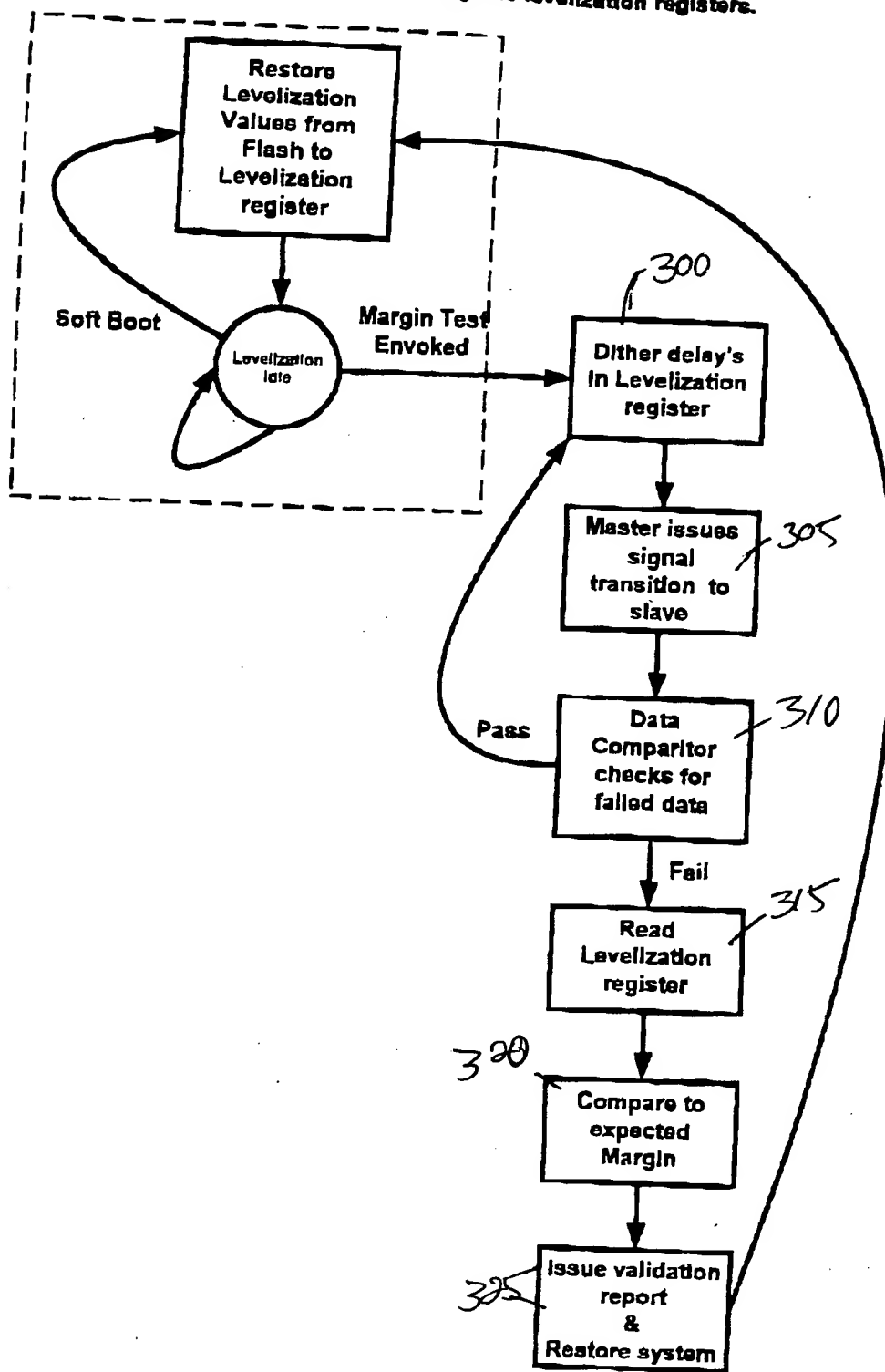


FIG 3

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